

INFORMATION DISCLOSURE CITATION
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Docket Number (Optional)

90

Application Number

Applicant(s)

Richard S. NORMAN et al.

Filing Date

Group Art Unit

U.S. PTO
09/870703
06/01/01

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
CU	1.	U.S. 5,008,878	16/04/1991	Ahmadi et al.			
	2.	U.S. Re. 34,755	11/10/1994	Eng et al.			
	3.	U.S. Re. 34,811	27/12/1994	Eng et al.			
	4.	U.S. 5,361,257	01/11/1994	Petersen Patent withdrawn			
CU	5.	U.S. 5,467,347	14/11/1995	Petersen			
CU	6.	U.S. 5,999,527	07/12/1999	Petersén			
CU	7.	U.S. 5,787,084	28/07/1998	Hoang et al.			
CU	8.	U.S. 5,043,980	27/08/1991	Day, Jr. et al.			
CU	9.	U.S. 6,144,662	07/11/2000	Colmant et al.			
CU	10.	U.S. 5,938,736	17/08/1999	Muller et al.			
CU	11.	U.S. 5,247,513	21/09/1993	Henrion et al.			

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	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
CU	12.	EP 0 680 173 A1	02/11/1995	EUROPE				

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CU	13.	Nick McKeown et al. "The Tiny Tera: a Packet Switch Core"; Departments of Electrical Engineering and Computer Science, Stanford University; August 1996; http://tiny-tera.stanford.edu/tiny-tera/index.html
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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
CW	14.	U.S. 6,111,856	29/08/2000	Huterer et al.			
CW	15.	U.s. 5,859,835	12/01/1999	Varma et al.			

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							YES	NO

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Anthony A. Das

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10/2/04

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13690

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*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
UD	1.	U.S. 5,377,182	12/27/1994	Monacos			
UD	2.	U.S. 5,278,548	01/11/1994	Haber			

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	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

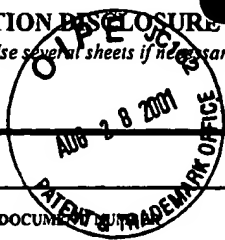
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER Anthony [Signature] DATE CONSIDERED 10/27/04

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June 1, 2001

Group Art Unit

2661

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CW	1.	U.S. 4,849,751	18/07/1989	Barber et al.			
CW	2.	U.S. 5,072,366	10/12/1991	Simcoe			
CW	3.	U.S. 4,955,020	04/09/1990	Stone et al.			

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CW	4.	French, R. Architectural Consideration for Internet Routers; retrieved from the internet guideline in file; Internet URL www.cise.ufl.edu/ rfrench, accessed July 23, 2001;
CW	5.	Joseph Desposito; Router-On-A-Chip Manages Network Traffic with Wire-Speed QoS; Electronic Design; May 1, 2000; pp 64-65-66;

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Cynthia L. Davis

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Cyrel Minkenberg et al. A combined Input and Output Queued Packet-Switched System Based on Prisma Switch-on-a-Chip Technology; Scalable High-Speed Switches/Routers with QoS Support; IBM Research, Zurich Research Laboratory; IEEE Communications Magazine; December 2000; pp 70-84;

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Chlld, J.; Bus-switching chip busts bandwidth barrier [on line]; Internet URL <http://www.computer-design.com/editorial/1995/06/directions/bus.html>; retrieved on March 15, 2001.

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PSID - Based Communications Switching [on line]; December 1997; Internet URL <http://www.icube.com/commsw.pdf>; retrieved on March 15, 2001; pp 1-14

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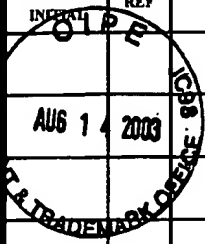
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2.		1 051 001 A2	11-08-2000	Europe				

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3.	Partial International Search Report; PCT/CA02/00810

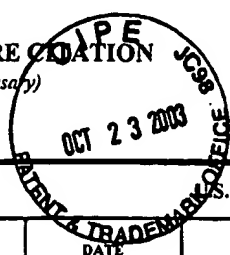
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CD	1.	U.S. 5,790,539	08-04-1998	Chao et al.			
CD	2.	U.S. 5,831,980	11-03-1998	Varma et al.			
CD	3.	U.S. 6,069,895	05-30-2000	Ayandeh			

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CD	5.	NOTANI H ET AL: "An 8*8 ATM switch LSI with shared multi-buffer architecture" PROCEEDINGS OF THE SYMPOSIUM ON VLSI CIRCUITS. SEATTLE, JUNE 4-6, 1992, SYMPOSIUM ON VLSI CIRCUITS, NEW YORK, IEEE, US, 4 June 1992 (1992-06-04), pages 74-75, XP010064987
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